AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method for enhancing effective timing margins and reliability of a digital system bus, comprising:

monitoring the digital system bus to determine a data flow between devices on the digital system bus; and

if an absence of data flow between devices on the digital system bus is detected;

generating a pseudo-data signal, and

~~transmission~~ transmitting the pseudo-data signal on the digital system bus, in order to keep the digital system bus active so that subsequent transmissions do not suffer from effects caused by an inactive digital system bus;

wherein keeping the digital system bus active provides a constant load that maintains the digital system bus at a nominal operating temperature, thereby mitigating temperature-induced effects on timing margins, transmission-line effects, and first pulse distortion effects caused by an idle system bus.

2. (Original) The method of claim 1, further comprising terminating the pseudo-data signal abruptly when the digital system bus is needed to transmit real data.

3. (Original) The method of claim 1, wherein the pseudo-data signal is a pre-determined pattern sequence.

4. (Original) The method of claim 1, wherein the pseudo-data signal is a continually changing pattern sequence generated by a pseudo-random generator.

5. (Original) The method of claim 1, wherein the pseudo-data signal is a continually changing pattern sequence generated based on previous transitions on the digital system bus to maintain a substantially equal number of high and low transitions on the digital system bus.

6. (Original) The method of claim 1, further comprising directing the pseudo-data signal to a trash bin address, wherein the trash bin address is not used by devices on the digital system bus.

7. (Original) The method of claim 1, further comprising generating an idle command in conjunction with the pseudo-data signal, wherein the idle command informs devices on the digital system bus not to use the pseudo-data signal.

8. (Currently amended) An apparatus that facilitates enhancing effective timing margins and reliability of a digital system bus, comprising:

a monitoring mechanism that is configured to monitor the digital system bus to determine a data flow between devices on the digital system bus;

a generating mechanism that is configured to generate a pseudo-data signal if an absence of data flow between devices on the digital system bus is detected; and

a transmission mechanism that is configured to broadcast the pseudo-data signal on the digital system bus, in order to keep

the digital system bus active so that subsequent transmissions do not suffer from effects caused by an inactive digital system bus ;

wherein keeping the digital system bus active provides a constant load that maintains the digital system bus at a nominal operating temperature, thereby mitigating temperature-induced effects on timing margins, transmission-line effects, and first pulse distortion effects caused by an idle system bus.

9. (Original) The apparatus of claim 8, further comprising a terminating mechanism that is configured to terminate the pseudo-data signal abruptly when the digital system bus is needed to transmit real data.

10. (Original) The apparatus of claim 8, wherein the pseudo-data signal is a pre-determined pattern sequence.

11. (Original) The apparatus of claim 8, further comprising a pseudo-random generator configured to generate a continually changing pattern sequence for the pseudo-data signal.

12. (Original) The apparatus of claim 8, wherein the pseudo-data signal is a continually changing pattern sequence generated based on previous transitions on the digital system bus to maintain a substantially equal number of high and low transitions on the digital system bus.

13. (Original) The apparatus of claim 12, wherein the pseudo-data signal is generated by software, wherein the software executes on a central processing unit associated with a host system.

14. (Original) The apparatus of claim 8, further comprising an addressing mechanism that is configured to direct the pseudo-data signal to a trash bin address, wherein the trash bin address is not used by devices on the digital system bus.

15. (Original) The apparatus of claim 8, further comprising an idle command generating mechanism that is configured to generate an idle command in conjunction with the pseudo-data signal, wherein the idle command informs devices on the digital system bus not to use the pseudo-data signal.

16. (Original) The apparatus of claim 8, wherein effects caused by the inactive digital system bus include a first pulse distortion effect caused by temperature and voltage changes associated with a first pulse after an idle period on the digital system bus.

17. (Original) The apparatus of claim 8, wherein effects caused by the inactive digital system bus include a power supply effect associated with the digital system bus returning to a constant load level after an idle period on the digital system bus.

18. (Original) The apparatus of claim 8, wherein effects caused by the inactive digital system bus include a transmission line mis-matching effect associated with signal reflections on the digital system bus caused by mis-matched impedance on the digital system bus.

19. (Original) The apparatus of claim 8, wherein effects caused by the inactive digital system bus include temperature effects associated with signal

driver transistors being held in a constant state of conduction during an idle period on the digital system bus.

20. (Original) The apparatus of claim 8, wherein the generating mechanism is further configured to generate the pseudo-data signal in a manner such that crosstalk is minimized across the digital system bus.

21. (Currently amended) A computer system that facilitates enhancing effective timing margins and reliability of a digital system bus, comprising:

a central processor unit coupled to the digital system bus;

a memory subsystem coupled to the digital system bus;

a monitoring mechanism that is configured to monitor the digital system bus to determine a data flow between the central processor unit and the memory subsystem on the digital system bus;

a generating mechanism that is configured to generate a pseudo-data signal if an absence of data flow between the central processor unit and the memory subsystem is detected; and

a transmission mechanism that is configured to broadcast the pseudo-data signal on the digital system bus, in order to keep the digital system bus active so that subsequent transmissions between the central processor unit and the memory subsystem do not suffer from effects caused by an inactive digital system bus ;

wherein keeping the digital system bus active provides a constant load that maintains the digital system bus at a nominal operating temperature, thereby mitigating temperature-induced effects on timing margins, transmission-line effects, and first pulse distortion effects caused by an idle system bus.